

IN THE CLAIMS

Please amend claims 11 and 16. The text of all pending claims, along with their current status indicators, is set forth below. This listing of claims replaces all previous listings.

1. (Original) A data amplifier comprising:
 - a plurality of helper flip-flops configured to receive data;
 - an isolation latch coupled to each of the plurality of helper flip-flops and configured to receive the data from each of the plurality of helper flip-flops;
 - an inverter loop coupled to each isolation latch and configured to hold at least a portion of the data for a period of time; and
 - an output driver coupled to each inverter loop and configured to transmit the at least a portion of data received from each inverter loop.
2. (Original) The data amplifier, as set forth in claim 1, wherein the plurality of helper flip-flops comprises four helper flip-flops.
3. (Original) The data amplifier, as set forth in claim 1, wherein each of the plurality of helper flip-flops is configured to receive a pair of data inputs and at least one enable signal.
4. (Original) The data amplifier, as set forth in claim 1, wherein each of the plurality of helper flip-flops is configured to transmit a pair of output data signals.

5. (Original) The data amplifier, as set forth in claim 1, wherein the plurality of helper flip-flops are configured to transmit a pair of output data signals to a shift register.

6. (Original) The data amplifier, as set forth in claim 1, wherein the plurality of helper flip-flops are configured to transmit a pair of output data signals to an output buffer.

7. (Original) The data amplifier, as set forth in claim 1, wherein a first half of the plurality of helper flip-flops is configured to transmit data at a first time and wherein a second half of the plurality of helper flip-flops is configured to transmit data at a second time.

8. (Original) The data amplifier, as set forth in claim 7, wherein the first half of the plurality of helper flip-flops transmits data periodically at alternating intervals from the second half of the plurality of helper flip-flops.

9. (Original) The data amplifier, as set forth in claim 2, wherein:

a first of the four helper flip-flops is configured to transmit data at a first time;

a second of the four helper flip-flops is configured to transmit data at a second time different from the first time;

a third of the four helper flip-flops is configured to transmit data at a third time different from the first time and the second time; and

a fourth of the four helper flip-flops is configured to transmit data at a fourth time different from the first time, the second time, and the third time.

10. (Original) The data amplifier as set forth in claim 9, wherein the first of the four helper flip-flops, the second of the four helper flip-flops, the third of the four helper flip-flops, and the fourth of the four helper flip-flops are configured to transmit in periodic succession.

11. (Currently amended) A data amplifier ~~comprising a plurality helper flip-flops~~ configured to receive data on a first data bus having a first bus width and configured to transmit data on a second bus having a second bus width, wherein the first bus width is greater than the second bus width, and wherein the data amplifier comprises a plurality of helper flip-flops configured to receive the data on the first bus and a plurality of logical devices configured to store, hold and deliver the data from the plurality of helper flip-flops onto the second bus in an alternating sequence.

12. (Original) The data amplifier, as set forth in claim 11, wherein the first bus width is two times greater than the second bus width.

13. (Original) The data amplifier, as set forth in claim 11, wherein the first bus width is four times greater than the second bus width.

14. (Original) The data amplifier, as set forth in claim 11, wherein the plurality of helper flip-flops is configured to receive four bits of data at a first time, to transmit two bits of the data at a second time, and to transmit two bits of the data at a third time different from the second time.

15. (Original) The data amplifier, as set forth in claim 11, wherein the second data bus comprises one of a 16-bit data bus and a 32-bit data bus.

16. (Currently Amended) A data amplifier ~~comprising a plurality helper flip-flops~~ configured to receive data on a first data bus having a first operating speed and configured to transmit data on a second bus having a second operating speed, wherein the second operating speed is greater than the first operating speed, and wherein the data amplifier comprises a plurality of helper flip-flops configured to receive the data on the first bus and a plurality of logical devices configured to store, hold and deliver the data from the plurality of helper flip-flops onto the second bus in an alternating sequence.

17. (Original) The data amplifier, as set forth in claim 16, wherein the second operating speed is two times greater than the first operating speed.

18. (Original) The data amplifier, as set forth in claim 16, wherein the second operating speed is four times greater than the first operating speed.

19. (Original) The data amplifier, as set forth in claim 16, wherein the plurality of helper flip-flops is configured to receive four bits of data at a first time, to transmit two bits of the data at a second time, and to transmit two bits of the data at a third time different from the second time.

20. (Original) The data amplifier, as set forth in claim 16, wherein the second operating speed comprises one of 200MHz and 400MHz.